Analysis of Aluminum-Nitride SOI for High-Temperature Electronics

Bryan A. Biegel (NASA Ames Research Center)
Mohamed Osman (Washington State University)
Zhiping Yu (Stanford University)

Outline

- **Background (why and what)**
- **Simulation Results**
  - **Leakage Current (OFF)**
  - **Subthreshold (OFF to ON)**
  - **High Current (ON)**
- **Conclusions**

biegel@nas .nasa.go v, http://science .nas.nasa.go v/~biegel

NASA Interest in High-Temp Electronics

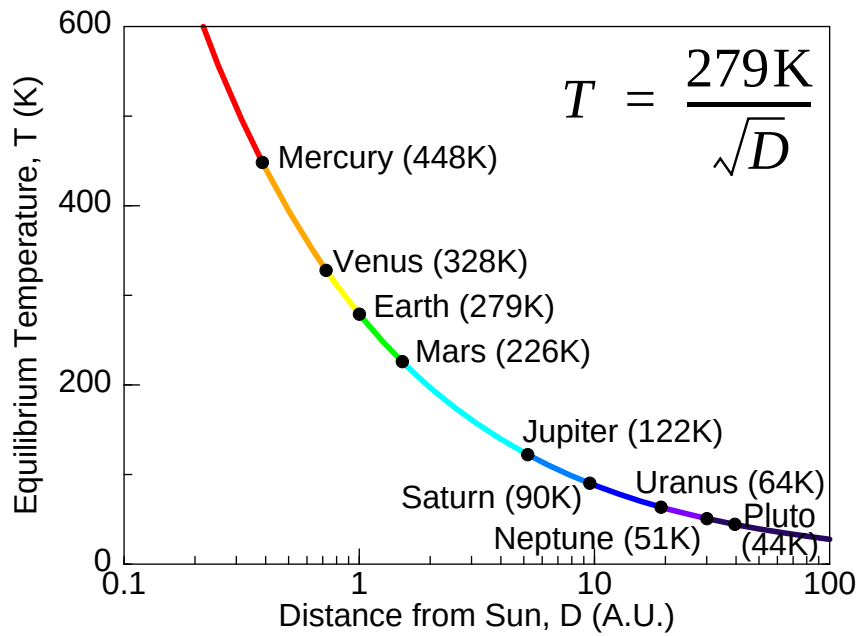
Spacecraft electronics temperature-sensitive:

- face hot and cold extremes
- constant thermal management required

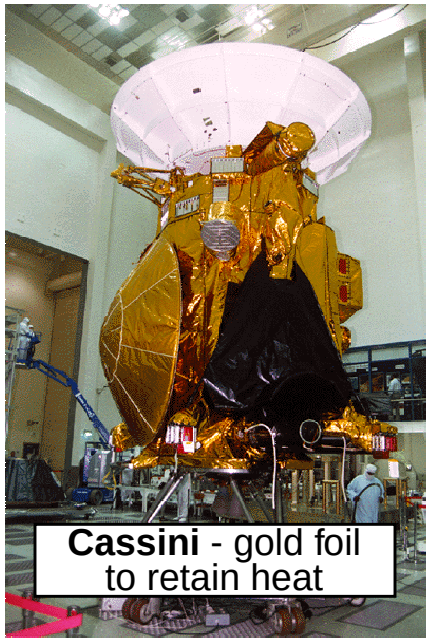
Future: sensors, comm during atmospheric entry

Earth orbit: 100K to 400K

Black-Body Sphere Temperature in Solar Orbit



Shuttle - open cargo bay to vent heat

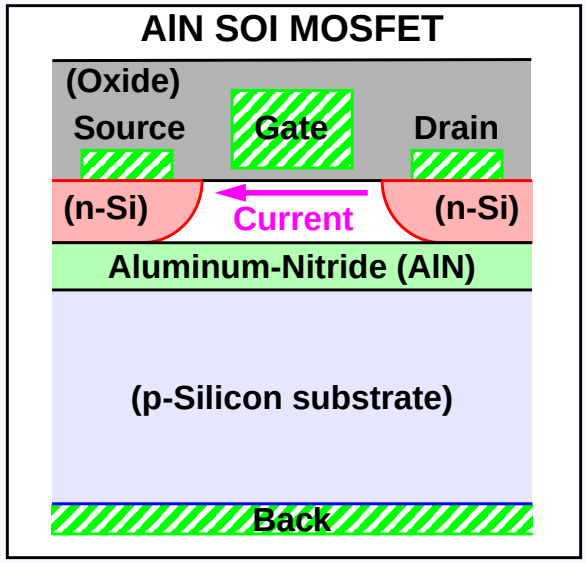


Cassini - gold foil to retain heat

Focus of This Work

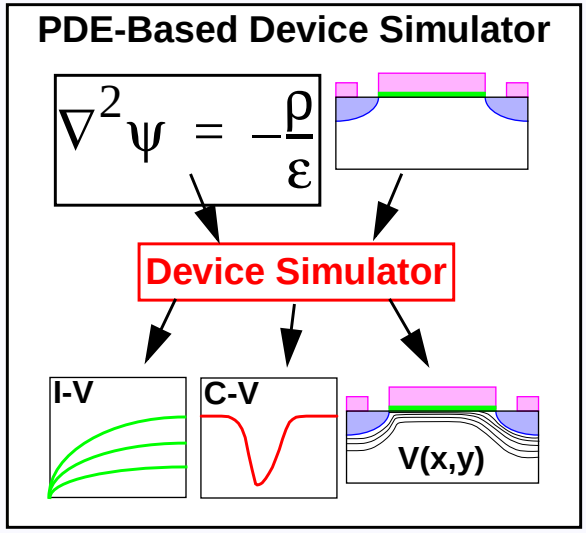
Electronics Technology (NASA application):

- Near-term ⇒ silicon-based CMOS
- Rad-hard ⇒ silicon-on-insulator (SOI)
- Minimize self-heating ⇒ Aluminum-Nitride insulator (high thermal cond.)
- High integration, low power ⇒ small
- High temp. operation ⇒ up to 500K



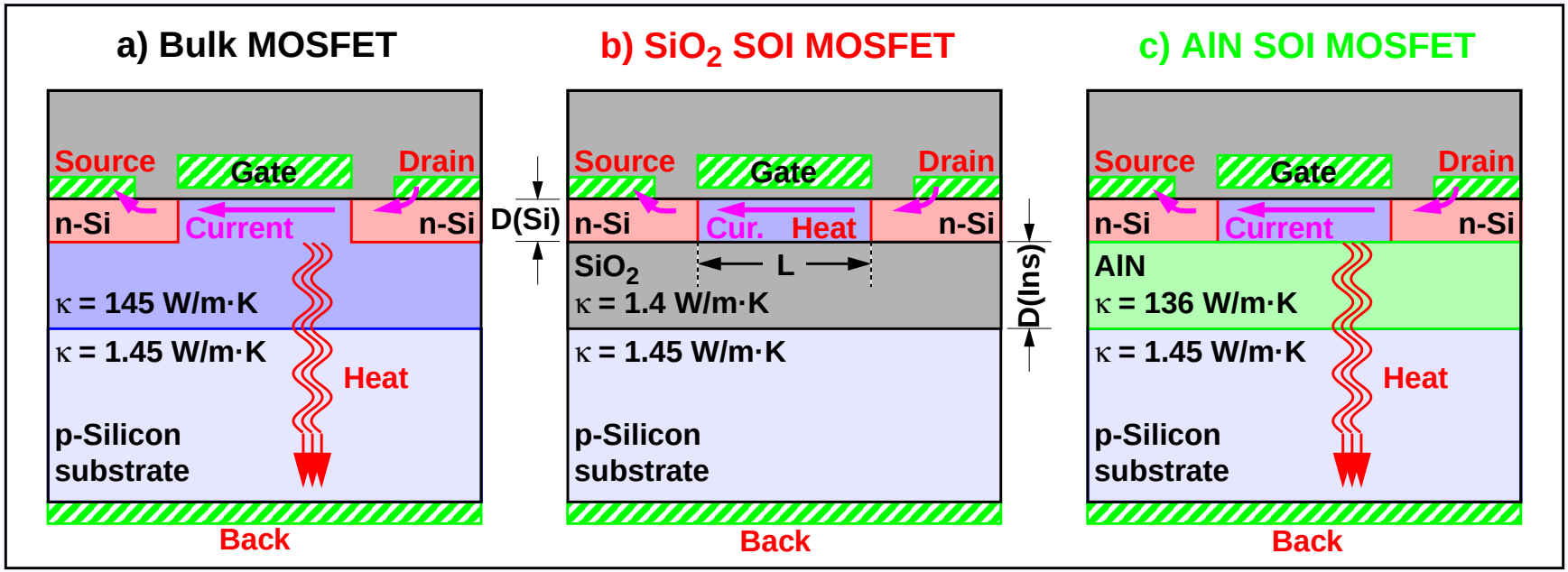
Simulation Technology:

- Thermal effects ⇒ electrothermal model
- Easily modifiable model ⇒ PDE solver (PROPHET)



Exploratory attempt to use a PDE solver for AlN-based SOI electrothermal simulation

Devices Simulated



Large: L=2.50µm, D(Si)=0.20µm, D(Ins)=0.6µm, D(ox)=10nm

Small: L=0.25µm, D(Si)=0.05µm, D(Ins)=0.2µm, D(ox)=4nm

Simulation region size: 5µm x 5µm

Main thermal contact: Back

Substrate: $\kappa = 0.01\kappa(\mathrm{Si})$ (~500 µm substrate)

Thermal contact at Source/Drain:

- approximate thermal transfer to top-side

Doping (Large & Small)

Epitaxial-Si: 1e17 p-type
Si Substrate: 5e15 p-type
Poly-Si Gate: 1e20 n-type
Source/Drain: 1e20 n-type

Electrothermal Model

Electrothermal Model (self-consistent charge and heat transport):

$$\nabla \cdot (\varepsilon \nabla \psi) = -q(p - n + N)$$

$$\frac{\partial n}{\partial t} = \nabla \cdot [D_n \nabla n - n\mu_n \nabla \psi] - R$$

$$\frac{\partial p}{\partial t} = \nabla \cdot [D_p \nabla p + p\mu_p \nabla \psi] - R$$

$$C_L \frac{\partial T_L}{\partial t} = \nabla \cdot (\kappa \nabla T_L) + \boldsymbol{J} \bullet \boldsymbol{E}$$

Solution v ariables:

- potential, ψ
- electron density , n
- hole density , p
- lattice temp , T_L

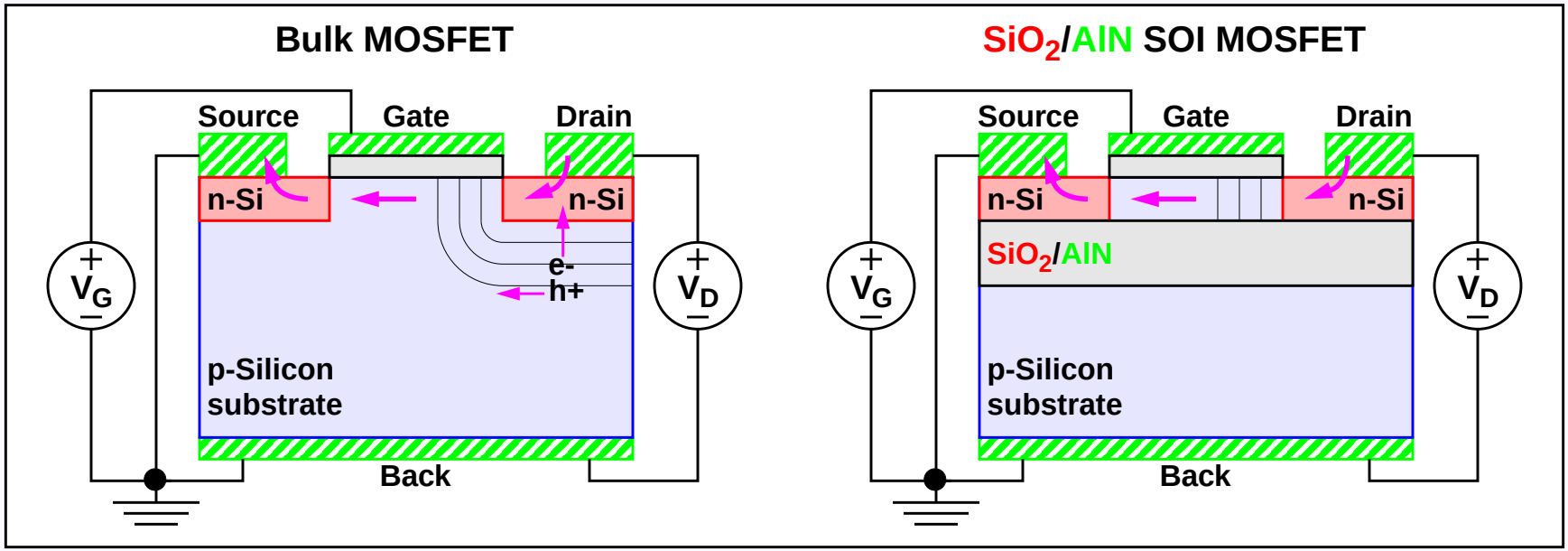
Temperature-dependence included:

- $D_n, D_p, \mu_n, \mu_p, \kappa, n_i, N_C, N_V, E_G$

Assumptions in this work:

- steady-state; T_{env} = 300K, 400K, 500K
- Maxwell-Boltzmann statistics (little change with Fermi-Dirac)

Drain Leakage Current Simulation



Ramp V_D at V_G = 0V (nominal OFF)

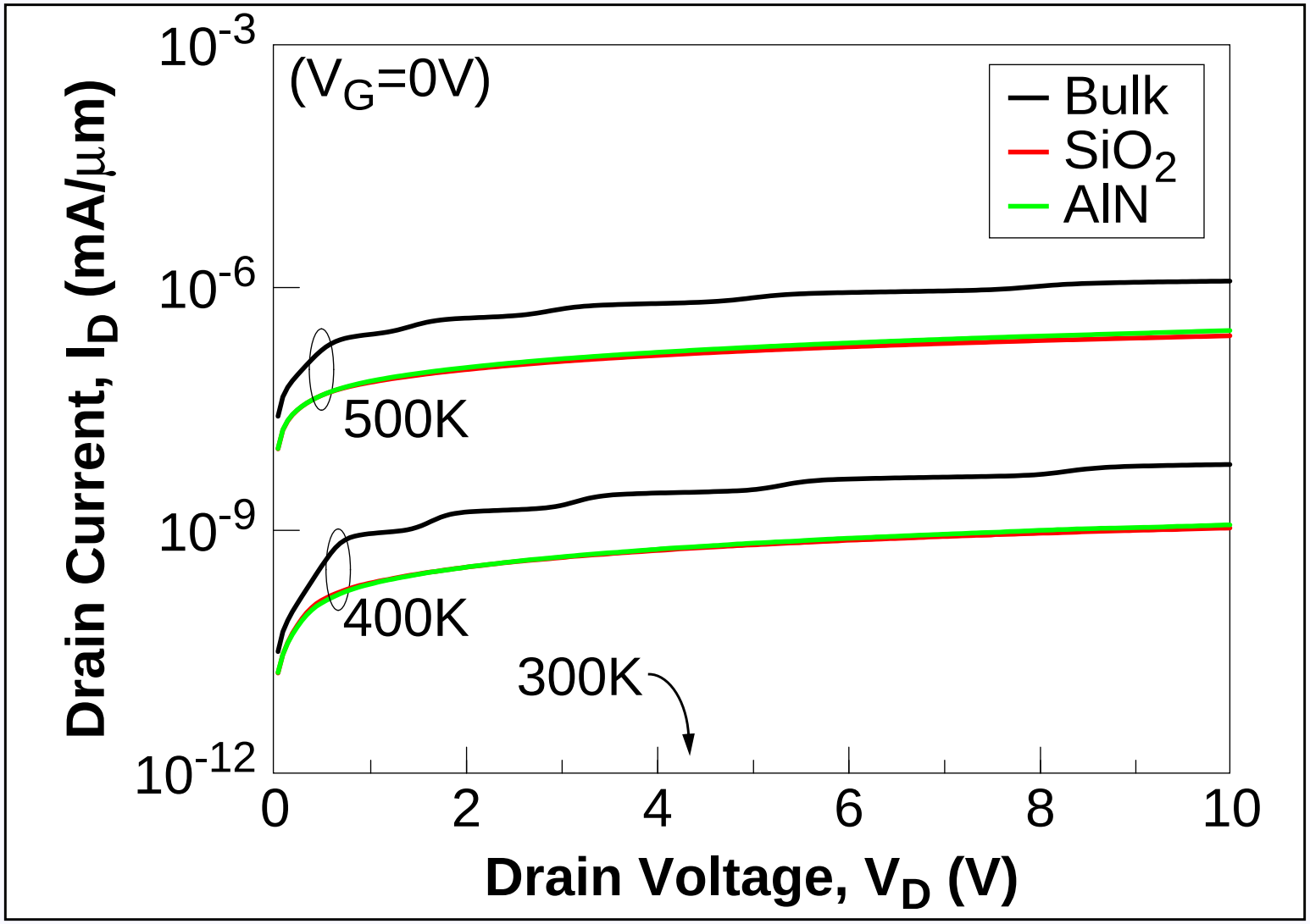
Large (L = 2.50 μm) MOSFETs: $0 \leq V_D \leq 10$

Small (L = 0.25 μm) MOSFETs: $0 \leq V_D \leq 3$

Expectations:

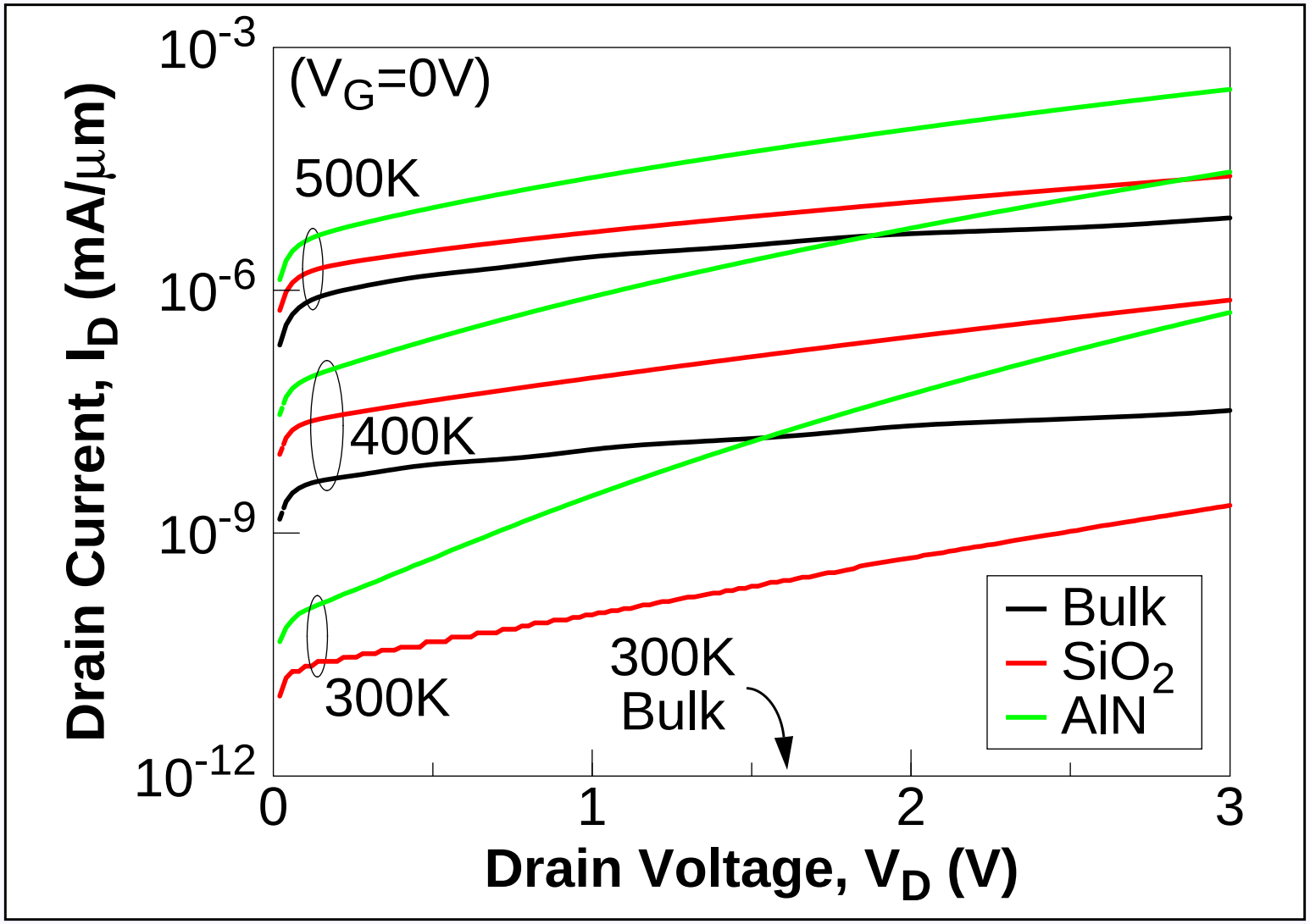
- No self-heating (low current): SiO_2 and AlN SOI same
- MOS: Higher leakage (junction EHP generation); worse at high T

Drain Leakage - Large MOSFETs



Expectations met: Bulk MOS has higher leakage; SiO_2 & AlN SOI same

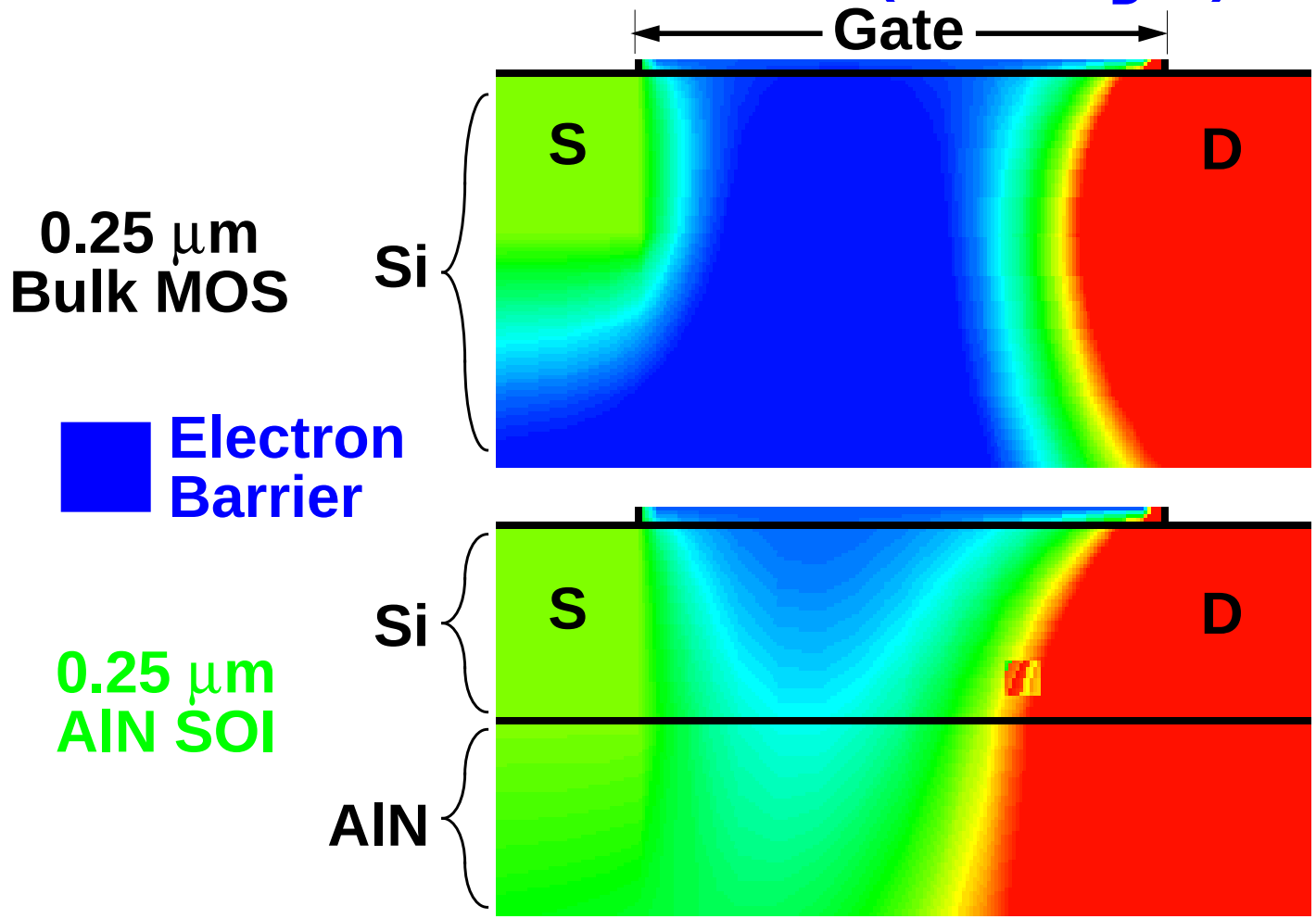
Drain Leakage - Small MOSFETs



Surprise: these short-channel SOIs have higher leakage, and differ...

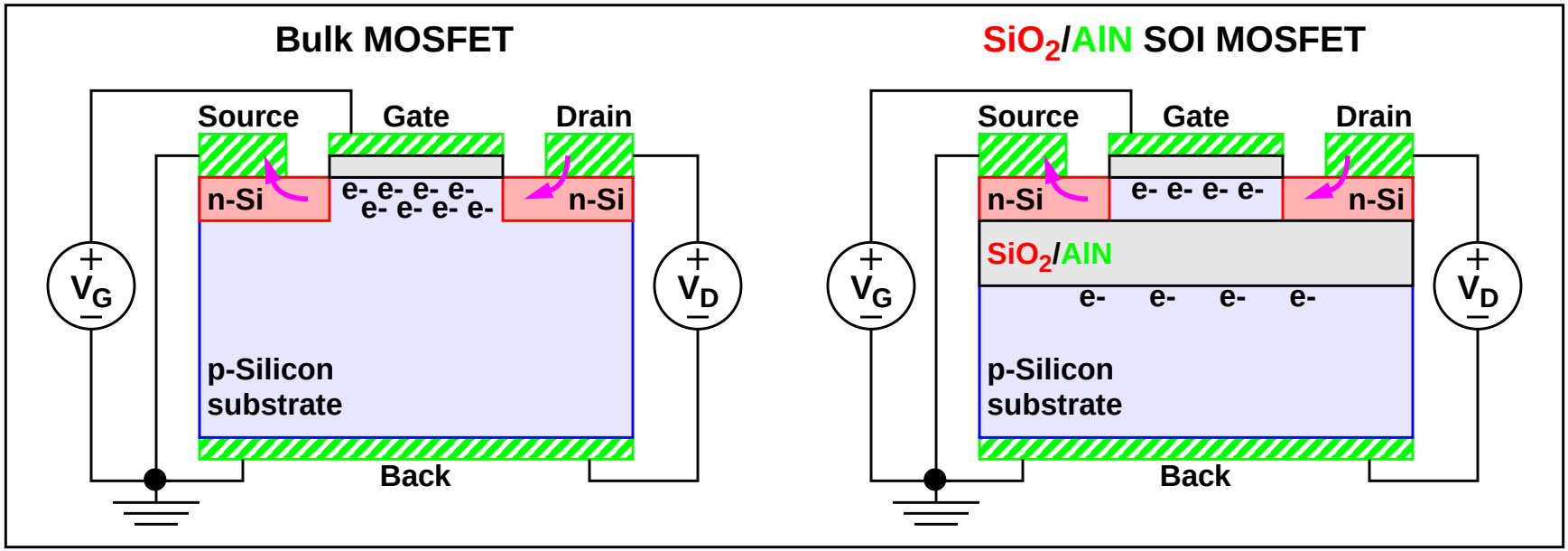
Drain Leakage - Small MOSFET Detail

2-D Electrostatic Potential (300K, V_D=3)



Small SOI devices fully-depleted: DIBL ⇒ higher OFF current

Subthreshold Current Simulation



Ramp V_G at V_D = 0.1V (turn-ON characteristic)

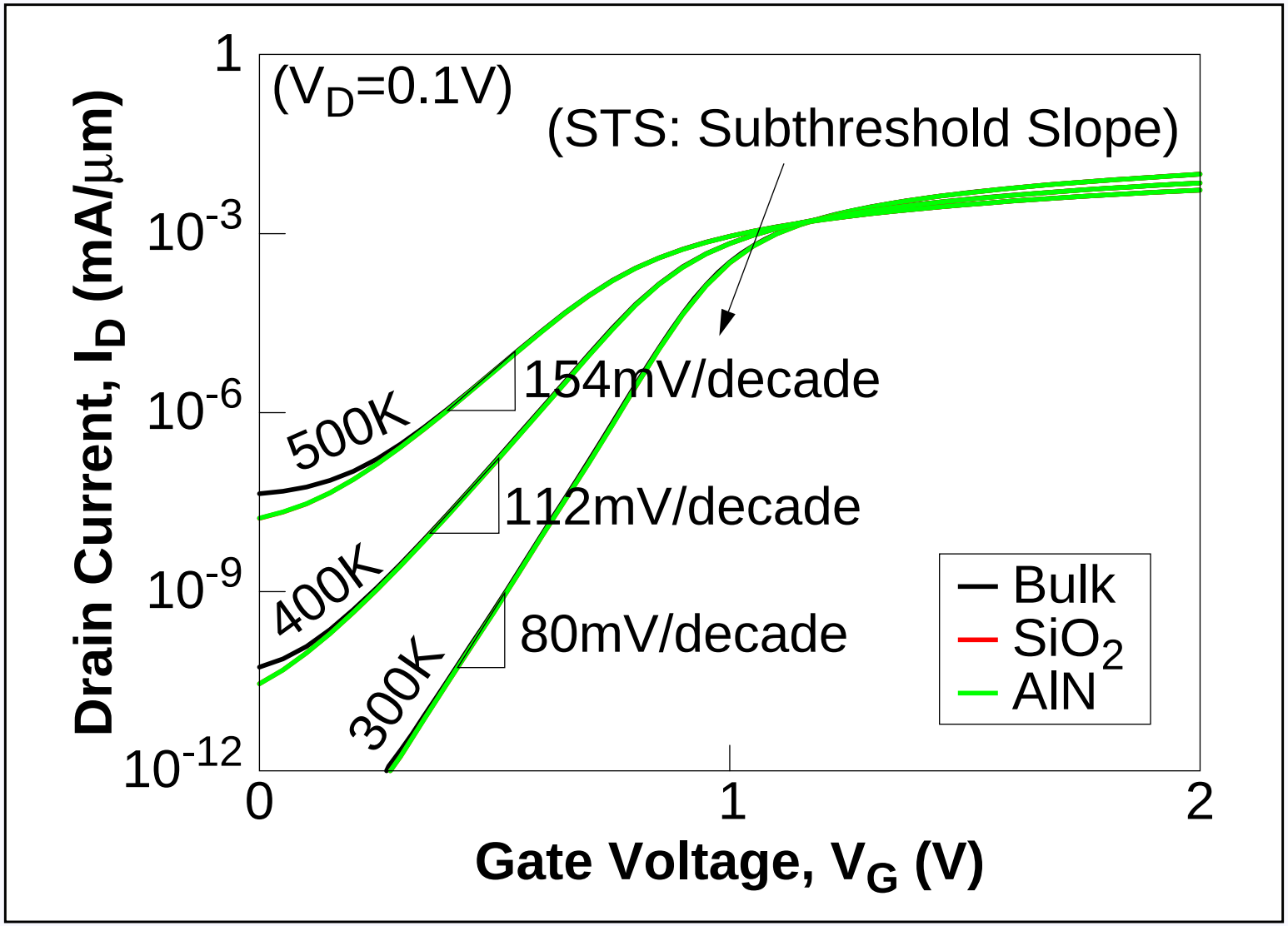
Large (L = 2.50 μm) MOSFETs: $0 \leq V_G \leq 10$

Small (L = 0.25 μm) MOSFETs: $0 \leq V_G \leq 3$

Expectations:

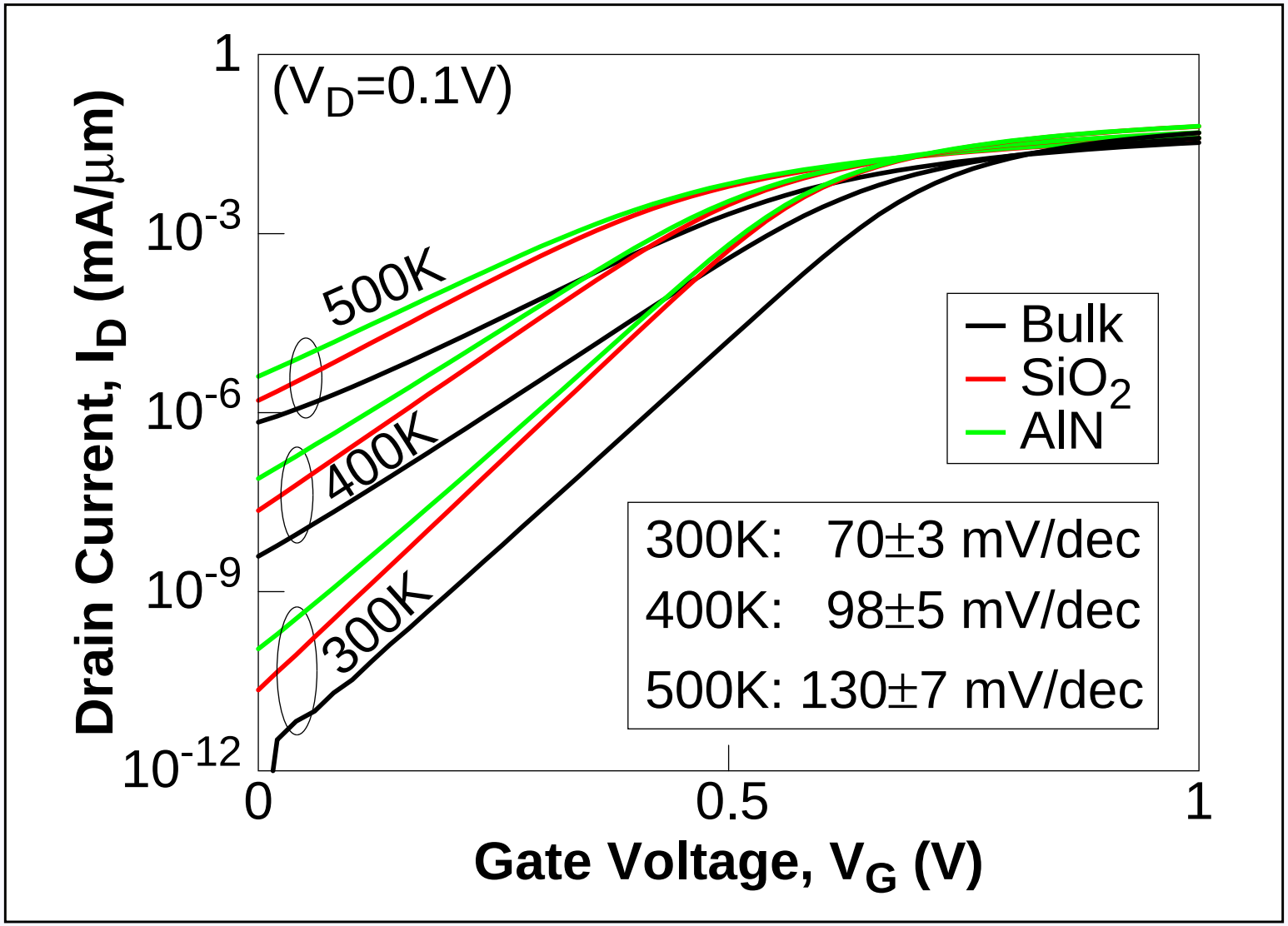
- No self-heating (low V_D): SiO_2 and AlN SOI same
- Large PD SOI: same as Bulk MOSFET (inversion layer in epi-Si)
- Small FD SOI: unknown...

Subthreshold Current - Large MOSFETs



Expectations met: Devices virtually identical in subthreshold

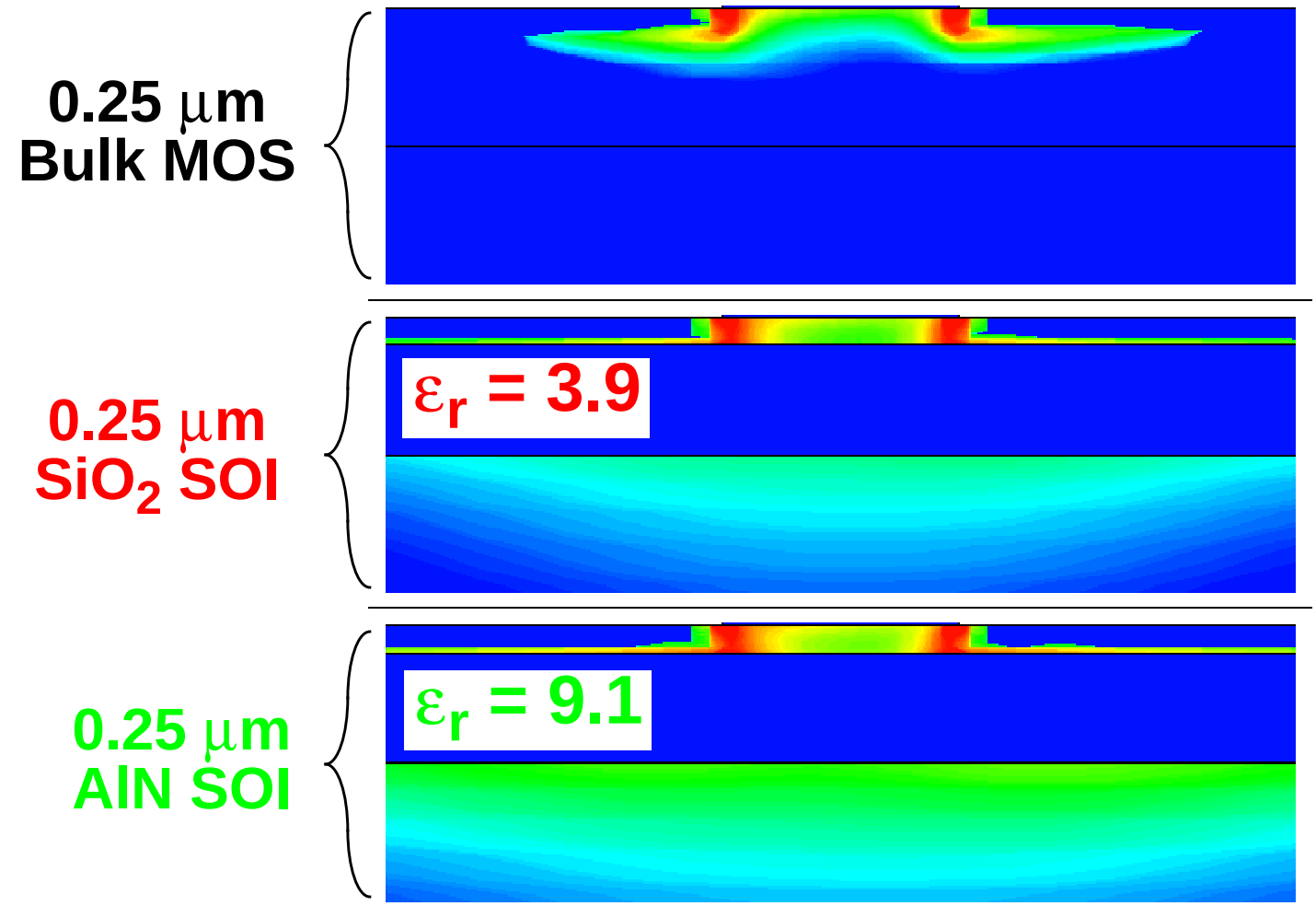
Subthreshold Current - Small MOSFETs



Surprise: SiO_2 SOI better STS than Bulk MOS; AlN SOI slightly worse

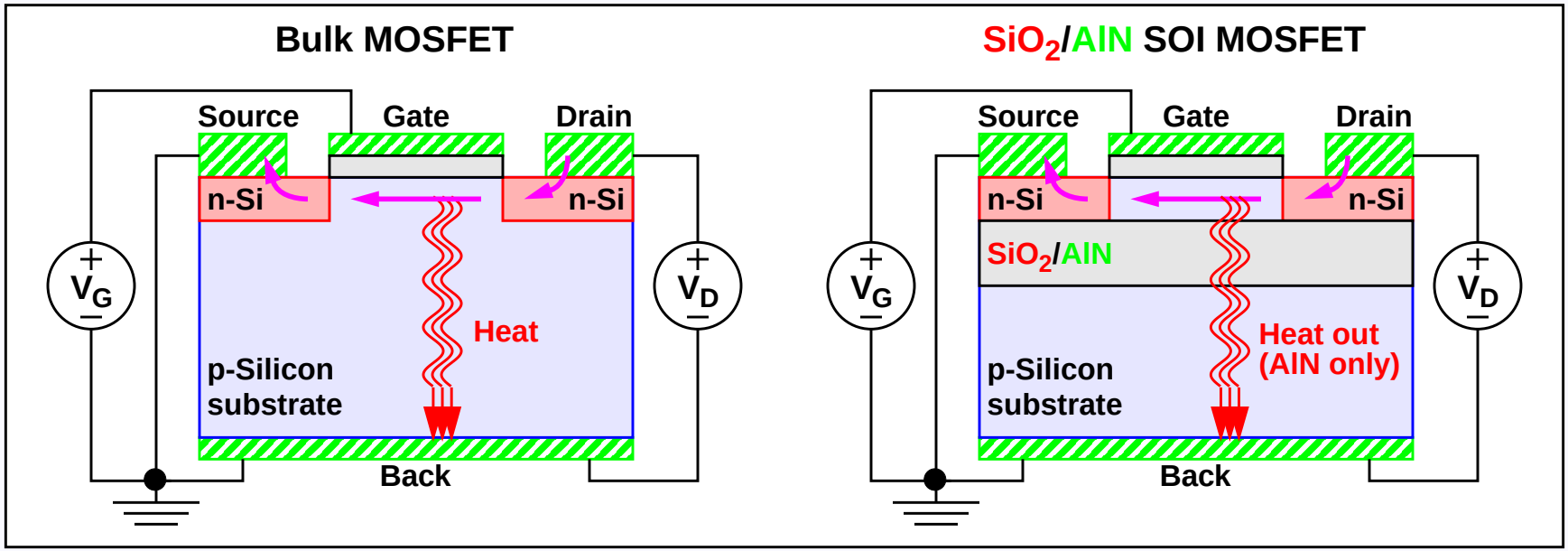
Subthreshold Current - Small MOSFET Detail

Change in Electron Density: 500K, 0.2V-0V



SiO_2 SOI has Δn in epi-SI; AlN SOI has significant Δn in substrate

High-Current (Device ON) Simulation



Ramp V_D at V_G = 3V (ON characteristic)

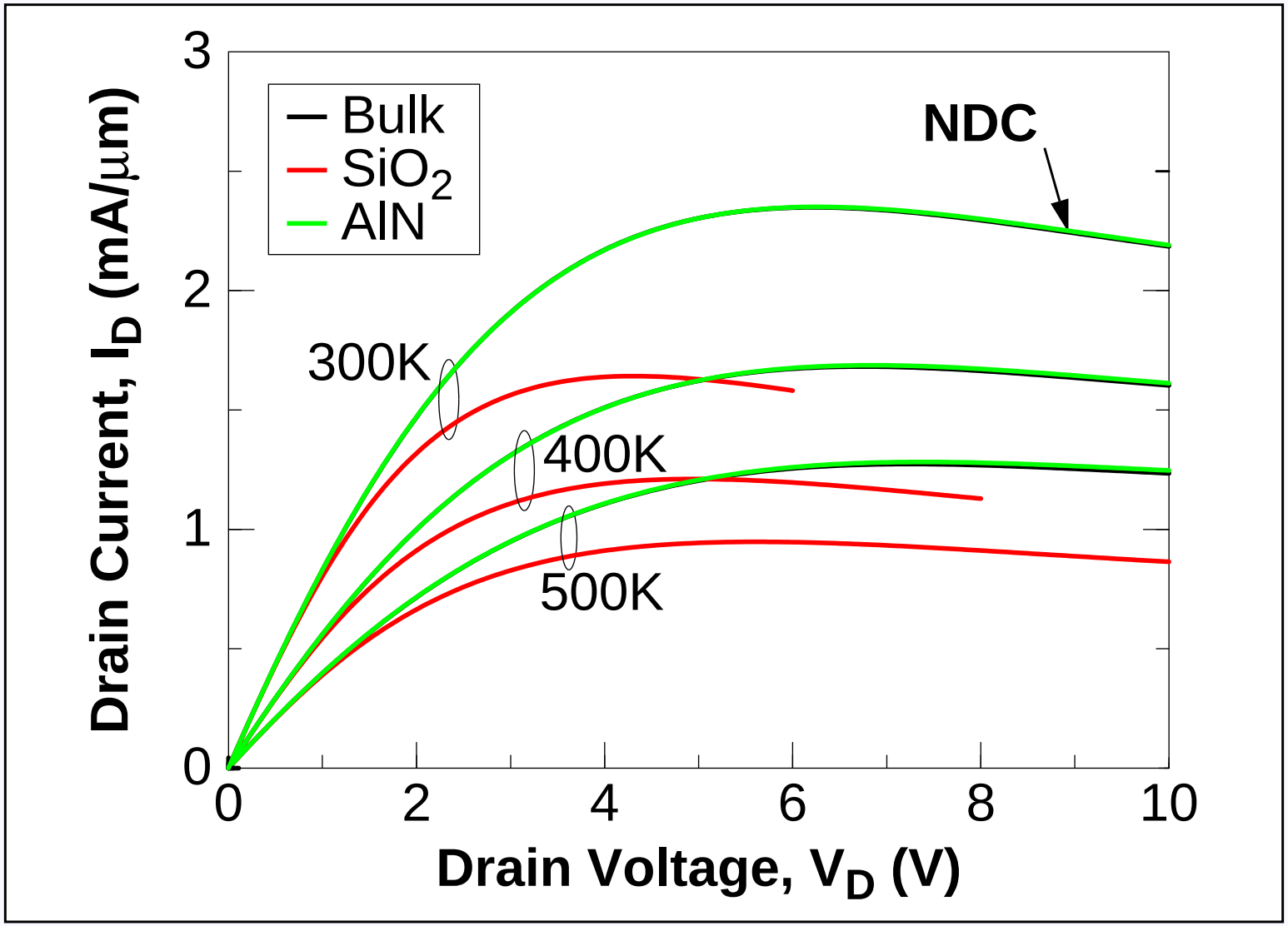
Long Channel (L = 2.5 µm) devices: $0 \leq V_D \leq 10$

Short Channel (L = 250 nm) devices: $0 \leq V_D \leq 3$

Expectations:

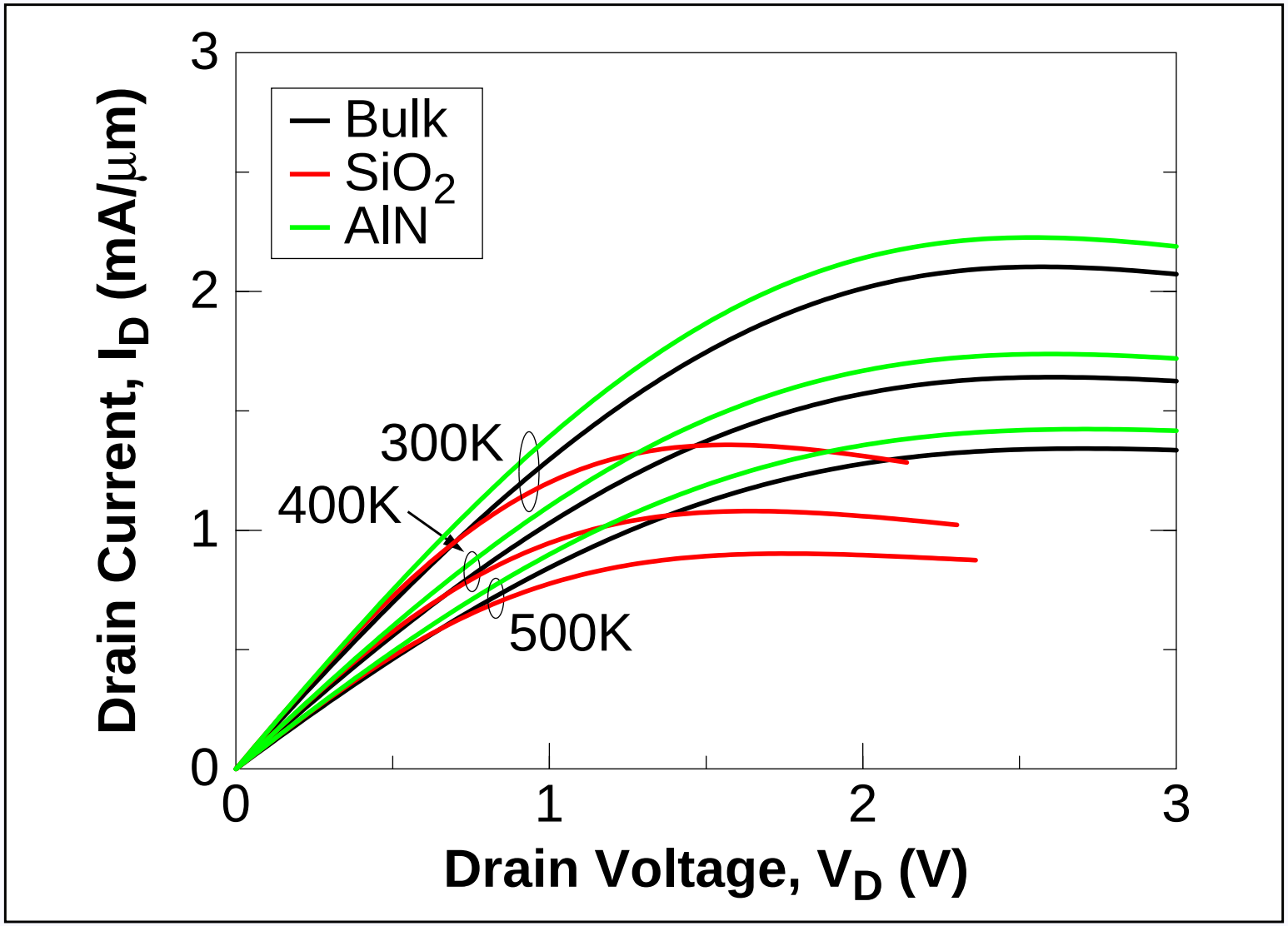
- Significant self-heating (high current and high V_D)
  - SiO_2 SOI: significantly reduced current drive
  - AlN SOI and Bulk MOS: similar self-heating

High Current - Large MOSFETs



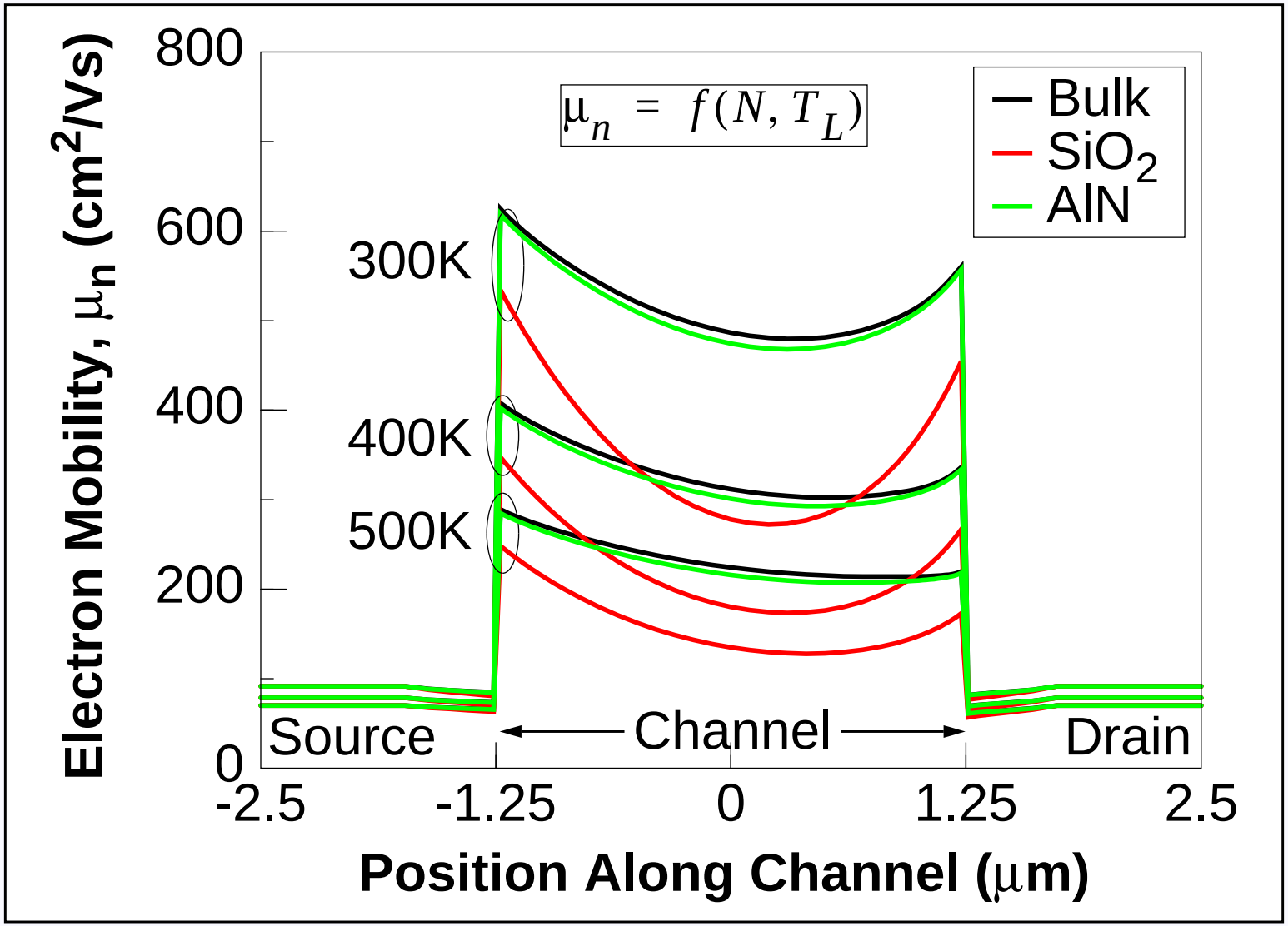
Self-heating significantly degrades SiO_2 SOI current; AlN SOI mitigates

High Current - Small MOSFETs



SiO_2 SOI self-heating effects (current decrease, NDC) increase with T_{env}

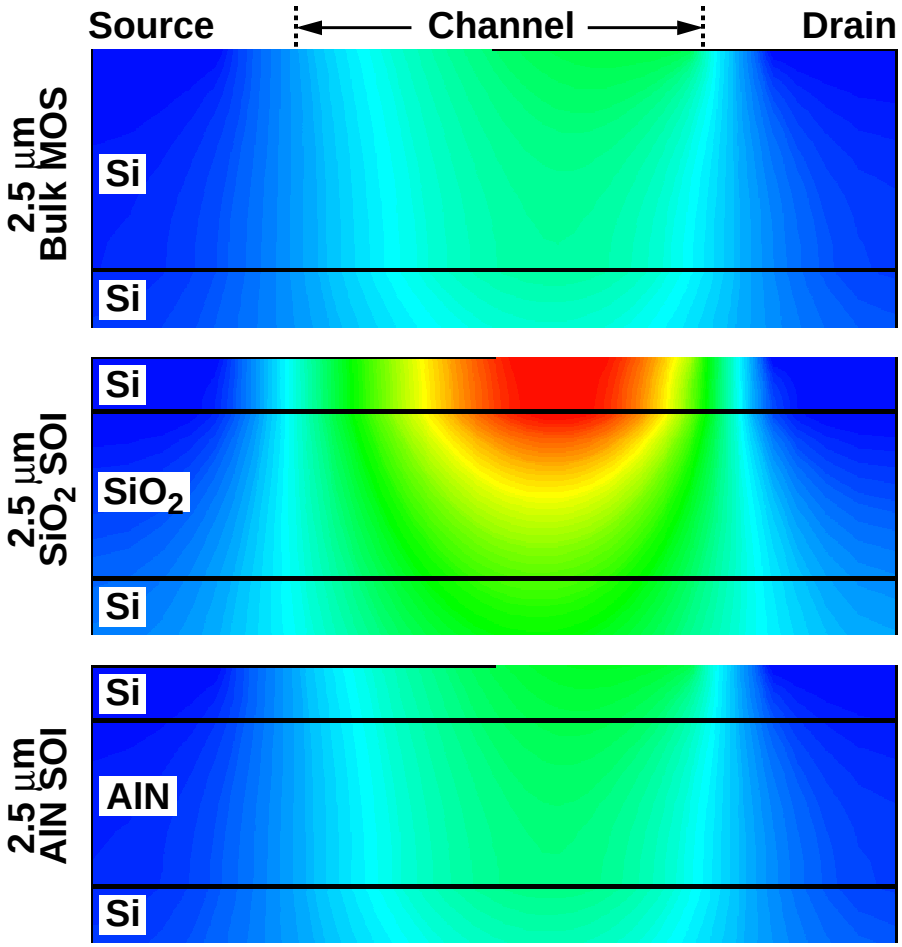
Mobility & Self-Heating - Large MOSFETs



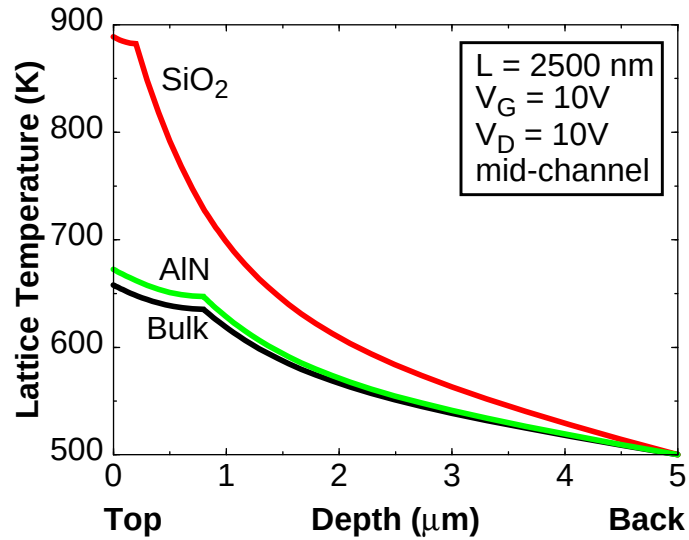
Carrier mobility degrades with temperature (self-heating and T_{env})

Temperature & Self-Heating - Large MOSFETs

2-D Temperature Plot (T_{env} = 500K)



500K Temperature Profiles



Summary:

- SiO_2-based SOI will melt itself at 500K T_{env}
- AlN SOI dramatically mitigates self-heating

Conclusions

Conclusions

- AlN eliminates self-heating penalty of SOI $\Rightarrow$ high-T silicon SOI
- PDE-solver device modeling works, even for electrothermal model
- Careful design of FD SOI required to optimize leakage, subthreshold
- High κ of AlN allows thick SOI insulator - new design flexibility

Future Work:

- optimize SOI device structure
- add impact ionization (kink/BJT effect)
- add body contact (minimize floating body effects)
- simulate full CMOS
- add quantum effects for ultra-small device simulation